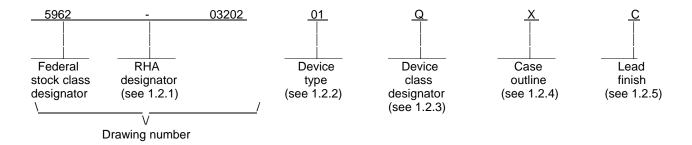
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1. SCOPE

- 1.1 <u>Scope</u>. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, choices of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.
 - 1.2 PIN. The PIN is as shown in the following example:



- 1.2.1 <u>RHA designator</u>. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.
 - 1.2.2 <u>Device type(s)</u>. The device type(s) identify the circuit function as follows:

Device type	Generic number 1/	Circuit function	Access time
01	82S181	1024 x 8-bit bipolar PROM	50 ns
02	82S181	1024 x 8-bit bipolar PROM	40 ns

1.2.3 <u>Device class designator</u>. The device class designator is a single letter identifying the product assurance level as follows:

Device class

Device requirements documentation

M Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A

Q or V Certification and qualification to MIL-PRF-38535

1.2.4 <u>Case outline(s)</u>. The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	<u>Terminals</u>		Package style
J	GDIP1-T24 or CDIP2-1	Γ24	24	dual-in-line package
K	GDFP2-F24 or CDFP3	-F24	24	flat package
L	GDIP3-T24 or CDIP4-1	Γ24	24	dual-in-line package
Χ	CQCC1-N32		32	rectangular chip carrier package
3	CQCC1-N28		28	square leadless chip carrier package

1.2.5 <u>Lead finish</u>. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

1/ Generic numbers are listed on the Standard Microcircuit Drawing Source Approval Bulletin at the end of this document and will also be listed in QML-38535 and MIL-HDBK-103 (see 6.6.2 herein).

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1.3 Absolute maximum ratings. 2/

Supply voltage range	-0.5 V dc to +7.0 V dc -1.5 V dc at -10 mA to +5.5 V dc -65°C to +150°C 1.1 mW
Lead temperature (soldering, 10 seconds)	+300°C
Thermal resistance, junction-to-case (θ_{JC}) $\underline{4}/$	See MIL-STD-1835
Junction temperature (T _J)	+175°C
DC voltage applied to outputs range (except	
during programming)	-0.5 V dc to +5.5 V dc maximum
DC voltage applied to outputs during programming	+21 V dc
Output current into outputs during programming	
(maximum duration of 1 second)	250 mA
DC input current range	-30 mA to +5.0 mA

1.4 Recommended operating conditions.

Supply voltage range (V _{CC})	4.5 V dc minimum to 5.5 V dc maximum
Minimum high level input voltage (V _{IH})	2.0 V dc
Maximum low level input voltage (V _{IL})	
Case operating temperature range (T _C)	-55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 <u>Government specification, standards, and handbooks</u>. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

DEPARTMENT OF DEFENSE

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

DEPARTMENT OF DEFENSE

MIL-STD-883 - Test Method Standard Microcircuits.

MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

HANDBOOKS

DEPARTMENT OF DEFENSE

MIL-HDBK-103 - List of Standard Microcircuit Drawings.

MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

- 2/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
- 3/ Must withstand the added P_D due to short circuit test, e.g., I_{OS}.
- 4/ Heat sinking is recommended to reduce the junction temperature.

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2.2 <u>Non-Government publications</u>. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents which are DoD adopted are those listed in the issue of the DoDISS cited in the solicitation. Unless otherwise specified, the issues of documents not listed in the DoDISS are the issues of the documents cited in the solicitation.

AMERICAN SOCIETY FOR TESTING AND MATERIALS (ASTM)

ASTM Standard F1192M-95 - Standard Guide for the Measurement of Single Event Phenomena (SEP) Induced by Heavy Ion Irradiation of Semiconductor Devices.

(Applications for copies of ASTM publications should be addressed to the American Society for Testing and Materials, 1916 Race Street, Philadelphia, PA 19103.)

ELECTRONICS INDUSTRIES ASSOCIATION (EIA)

JEDEC Standard EIA/JESD78 - IC Latch-Up Test.

(Applications for copies should be addressed to the Electronics Industries Association, 2500 Wilson Boulevard, Arlington, VA 22201.)

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents also may be available in or through libraries or other informational services.)

2.3 <u>Order of precedence</u>. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

- 3.1 <u>Item requirements</u>. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.
- 3.2 <u>Design, construction, and physical dimensions</u>. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.
 - 3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein.
 - 3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.
 - 3.2.3 Truth table(s).
- 3.2.3.1 <u>Unprogrammed devices</u>. Testing to the applicable truth table see figure 3 herein, shall be used for unprogrammed devices for contracts involving no altered item drawing. When testing is required in 4.4 herein, the devices shall be programmed by the manufacturer prior to test, in a checkerboard pattern (a minimum of 50 percent of the total number of bits programmed) or to any altered item drawing pattern which includes at least 25 percent of the total number of bits programmed.
- 3.2.3.2 <u>Programmed devices</u>. The truth table or test vectors for programmed devices shall be as specified by an attached altered item drawing.
- 3.2.4 <u>Switching test circuit and waveforms</u>. The switching test circuit and waveforms diagram shall be as specified on figure 3.
- 3.3 <u>Electrical performance characteristics and postirradiation parameter limits</u>. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

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- 3.4 <u>Electrical test requirements</u>. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table I.
- 3.5 <u>Marking</u>. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.
- 3.5.1 <u>Certification/compliance mark</u>. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.
- 3.6 <u>Certificate of compliance</u>. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.
- 3.7 <u>Certificate of conformance</u>. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.
- 3.8 <u>Notification of change for device class M.</u> For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-PRF-38535, appendix A.
- 3.9 <u>Verification and review for device class M.</u> For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.
- 3.10 <u>Microcircuit group assignment for device class M</u>. Device class M devices covered by this drawing shall be in microcircuit group number 14 (see MIL-PRF-38535, appendix A).
- 3.11 <u>Processing options</u>. Since the device is capable of being programmed by either the manufacturer or the user to result in a wide variety of configurations; two processing options are provided for selection in the contract, using an altered item drawing.
- 3.11.1 <u>Unprogrammed device delivered to the user</u>. All testing shall be verified through group A testing as defined in 4.4.1 and table IIA. It is recommended that users perform subgroups 7 and 9 after programming to verify the specific program configuration.
- 3.11.2 <u>Manufacturer-programmed device delivered to the user</u>. All testing requirements and quality assurance provisions herein, including the requirements of the altered item drawing, shall be satisfied by the manufacturer prior to delivery.

4. QUALITY ASSURANCE PROVISIONS

- 4.1 <u>Sampling and inspection</u>. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.
- 4.2 <u>Screening</u>. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.
 - 4.2.1 Additional criteria for device class M.
 - a. Delete the sequence specified as initial (preburn-in) electrical parameters through interim (postburn-in) electrical parameters of method 5004 and substitute lines 1 through 6 of table IIA herein.

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- The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.
 - (1) Dynamic burn-in for device class M (method 1015 of MIL-STD-883, test condition C or D; for circuit, see 4.2.1b herein).
- c. Interim and final electrical test parameters shall be as specified in table IIA herein.

4.2.2 Additional criteria for device classes Q and V.

- a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.
- b. Interim and final electrical test parameters shall be as specified in table IIA herein.
- Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.
- 4.3 <u>Qualification inspection for device classes Q and V.</u> Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).
- 4.4 <u>Conformance inspection</u>. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535 appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

- a. Tests shall be as specified in table IIA herein.
- b. Subgroups 5 and 6 of table I of method 5005 of MIL-STD-883 shall be omitted.
- c. Devices shall be tested for programmability and ac performance compliance to the requirements of group A, subgroups 9, 10, and 11. Either of two techniques is acceptable:
 - (1) Testing the entire lot using additional built-in test circuitry that allows the manufacturer to verify programmability and ac performance without programming the user array. If this is done, the resulting test patterns shall be verified on all devices during subgroups 9, 10, and 11, group A testing in accordance with the sampling plan specified in MIL-STD-883, method 5005.
 - (2) If such compliance cannot be tested on an unprogrammed device, a sample shall be selected to satisfy programmability requirements prior to performing subgroups 9, 10, and 11. Twelve devices shall be submitted to programming (see 3.2.3.2). If more than two devices fail to program, the lot shall be rejected. At the manufacturer's option, the sample may be increased to 24 total devices with no more than 4 total device failures allowable. Ten devices from the programmability sample shall be submitted to the requirements of group A, subgroups 9, 10, and 11. If more than two devices fail, the lot shall be rejected. At the manufacturer's option, the sample may be increased to 20 total devices with no more than 4 total device failures allowable.

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TABLE I. Electrical performance characteristics.

Test	Symbol	-55°C ≤ T ₀	litions _C ≤ +125°C _{CC} ≤ 5.5 V	Group A subgroups	Device type	Liı	Unit	
			vise specified			Min	Max	
Output high voltage	V _{OH}	$V_{CC} = 4.5 \text{ V}, \text{ I}_{H}$ $V_{IH} = 2.0 \text{ V}, \text{ V}$		1, 2, 3	All	2.4		V
Output low voltage	V _{OL}	$V_{CC} = 4.5 \text{ V}, \text{ I}_{H}$ $V_{IH} = 2.0 \text{ V}, \text{ V}$		1, 2, 3			.5	V
Input high level current	Іін	V _{CC} = 5.5 V, \	/ _{IN} = 5.5 V	1, 2, 3			50	μΑ
Input high level current	I _{IH2}	V _{CC} = 5.5 V, \	$I_{IN} = 4.5 \text{ V}$	1, 2, 3	-		100	μΑ
Input low level current	I _{IL}	V _{CC} = 5.5 V, \	$I_{IN} = 0.5 \text{ V}$	1, 2, 3		-1.0	-250	μΑ
Power supply current	Icc	V _{CC} = 5.5 V, \	V _{CC} = 5.5 V, V _{IN} = 0.0 V		-		185	mA
Input clamp voltage	V _{IC}	V _{CC} = 4.5 V, I	_{IN} = -10 mA	1, 2, 3	-		-1.5	V
High output leakage current	I _{OZH}	$V_{CC} = 5.5 \text{ V}$ $V_{IH} = 2.0 \text{ V}$	V _O = 5.2 V	1, 2, 3	-		100	μА
	I _{OZL}	V _{IL} = 0.8 V	V _O = 0.5 V				-100	
Output short circuit current	los	$V_{CC} = 5.5 \text{ V}, \text{ V}_{IH} = 2.0 \text{ V}, \text{ V}$		1, 2, 3		-15	-100	mA
Functional tests		See Table II a 3/ of Table II	and footnote	7, 8				
Address access time	t _{AVQV}	C _L = 30 pF		9, 10, 11	01		50	ns
		See figures 3	and 4		02		40	
Enable access time	t _{EVQV}	See figures 3	and 4 <u>2</u> /	9, 10, 11	01		30	ns
					02		25	
Enable recovery time	t _{EVQZ}	See figures 3	and 4 <u>2</u> /	9, 10, 11	01		30	ns
					02		25	

^{1/} Not more than one output should be shorted at a time and the duration of the short circuit condition should not exceed one second.

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^{2/} t_{EXQV} is tested with C_L = 30 pF to the 1.5 V level; S1 is open for high impedance to high tests and closed for high impedance to low tests. t_{EXQZ} is tested with C_L = 5 pF. High to high impedance tests are made with S1 open to an output voltage of V_{OH} - 0.5 V. Low to high impedance tests are made with S1 closed to the V_{OL} + 0.5 V level.

Device Types	All			
Case Outlines	J, K, L	3	Х	
Terminal	Terminal	Terminal	Terminal	
Number	Symbol	Symbol	Symbol	
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17	A7 A6 A5 A4 A3 A2 A1 A0 Q0 Q1 Q2 GND Q3 Q4 Q5 Q6 Q7 CE4	NC A7 A6 A5 A4 A3 A2 A1 A0 NC Q0 Q1 Q2 GND NC Q3 Q4 Q5	NC NC A7 A6 A5 A4 A3 A2 A1 A0 NC Q0 Q1 Q2 NC GND Q3 NC	
19	CE3	Q6	Q4	
20	$\overline{CE \ 2}$	Q7	Q5	
21	CE 1	NC	Q6	
22	A9	CE4	Q7	
23	A8	CE3	NC	
24	VCC	$\overline{CE 2}$	CE4	
25		$\overline{CE1}$	CE3	
26		A9	$\overline{CE \ 2}$	
27		A8	NC_	
28		VCC	\overline{CE} 1	
29			A9	
30			A8	
31			NC	
32			VCC	

Symbol CS and E are one in the same.

FIGURE 1. <u>Terminal connections</u>.

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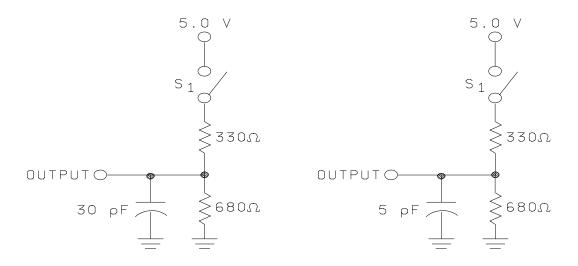
Read modes

CE 1	$\overline{CE2}$	CE3	CE4	A9A0	Q7Q0
L	L	Н	Н	Х	Data out
L	Н	н	н	X	Three-state
Н	L	Н	Н	Х	Three-state
Н	Н	L	Н	X	Three-state
Н	Н	L	L	Х	Three-state

NOTES:

X can be L or H.

FIGURE 2. Truth table.



Output load for all switching tests except t_{EXQV} .

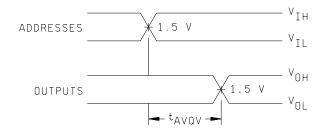
Output load for t_{EXQZ} .

NOTES:

- 1. All device test loads should be located within two inches of device output pin.
- 2. S_1 is open for output data high to high-Z and high-Z to output data high tests. S_1 is closed for all other switching tests.
- 3. The load capacitance includes all stray and fixture capacitance.

FIGURE 3. Output load circuit or equivalent.

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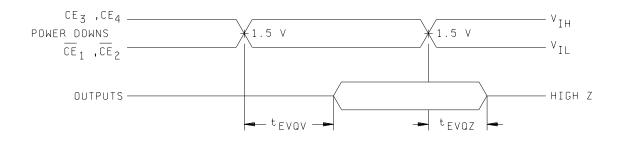


FIGURE 4. Read cycle waveform.

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TABLE IIA. Electrical test requirements. 1/2/3/4/5/6/7/

Line no.	Test requirements	Subgroups (in accordance with MIL-STD-883, TM 5005, table I)	(in accord	roups dance with 535, table III)
		Device class M	Device class Q	Device class V
1	Interim electrical parameters (see 4.2)	1	1, 7, 9	1, 7, 9
2	Static burn-in (method 1015)	Not required	Not required	Not required
3	Same as line 1			1*, 7* Δ
4	Dynamic burn-in (method 1015)	Required	Required	Required
5	Same as line 1			1*, 7* Δ
6	Final electrical parameters for unprogrammed devices (see 4.2)	1*, 2, 3, 7*, 8A, 8B	1*, 2, 3, 7*, 8A, 8B	1*, 2, 3, 7*, 8A, 8B,
	Final electrical parameters for programmed devices (see 4.2)	1*, 2, 3, 7*, 8A, 8B, 9	1*, 2, 3, 7*, 8A, 8B, 9	1*, 2, 3, 7*, 8A, 8B, 9
7	Group A test requirements (see 4.4)	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11
8	Group C end-point electrical parameters (see 4.4)	1,2, 3, 7, 8A, 8B	1,2, 3, 7, 8A, 8B	1, 2, 3, 7, 8A, 8B, 9, 10, 11 Δ
9	Group D end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9	1, 7, 9
10	Group E end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9	1, 7, 9

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 $[\]underline{1}/$ Blank spaces indicate tests are not applicable. $\underline{2}/$ Any or all subgroups may be combined when using high-speed testers.

^{3/} Subgroups 7 and 8 functional tests shall verify the truth table. For unprogrammed devices delivered to the user it is recommended that users perform subgroups 7 and 9 after programming to verify the specific program configuration.

 $[\]underline{4}/$ * indicates PDA applies to subgroup 1 and 7. $\underline{5}/$ ** see 4.4.1c.

^{6/} Δ indicates delta limit (see table IIB) shall be required where specified, and the delta values shall be computed with reference to the zero hour electrical parameters (see line 1).

TABLE IIB. Delta limits at +25°C.

Parameter <u>1</u> /	Device types
	All
I _{OZL} and I _{OZH}	± 10% of specified value in table I

- 1/ The above parameter shall be recorded before and after the required burn-in and life tests to determine the delta (Δ).
- 4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.
- 4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:
 - a. Test condition D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.
 - b. $T_A = +125^{\circ}C$, minimum.
 - c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.
- 4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.
 - 4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.
- 4.4.4 <u>Group E inspection</u>. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device classes M, Q and V shall be as specified in MIL-PRF-38535. End-point electrical parameters shall be as specified in table IIA herein.
- 4.5 <u>Delta measurements for device class V.</u> Delta measurements, as specified in table IIA, shall be made and recorded before and after the required burn-in screens and steady-state life tests to determine delta compliance. The electrical parameters to be measured, with associated delta limits are listed in table IIB. The device manufacturer may, at his option, either perform delta measurements or within 24 hours after burn-in perform final electrical parameter tests, subgroups 1, 7, and 9.
- 4.6 <u>Programming procedures</u>. The programming procedures shall be as specified by the device manufacturer and shall be made available upon request.
 - 5. PACKAGING
- 5.1 <u>Packaging requirements</u>. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.
 - 6. NOTES
- 6.1 <u>Intended use</u>. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.
- 6.1.1 <u>Replaceability</u>. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.
 - 6.1.2 Substitutability. Device class Q devices will replace device class M devices.
- 6.2 <u>Configuration control of SMD's</u>. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

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- 6.3 <u>Record of users</u>. Military and industrial users should inform Defense Supply Center Columbus when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.
- 6.4 <u>Comments</u>. Comments on this drawing should be directed to DSCC-VA , Columbus, Ohio 43216-5000, or telephone (614) 692-0547.
- 6.5 <u>Abbreviations, symbols, and definitions</u>. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.
 - 6.6 Sources of supply.
- 6.6.1 <u>Sources of supply for device classes Q and V</u>. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.
- 6.6.2 <u>Approved sources of supply for device class M.</u> Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

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STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 03-01-23

Approved sources of supply for SMD 5962-03202 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535.

Standard microcircuit drawing PIN <u>1</u> /	Vendor CAGE number	Vendor similar PIN <u>2</u> /
5962-0320201QXA	0C7V7	82S181A-50/QXA
5962-0320202QXA	<u>3</u> /	82S181A-40/QXA

- 1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed, contact the Vendor to determine its availability.
- 2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
- 3/ Not available from an approved source.

Vendor CAGEVendor namenumberand address

0C7V7 Qualified Parts Laboratory, Inc.

3605 Kifer Road Santa Clara, CA 95051

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.